

What is claimed is:

1. A method of providing electrostatic discharge protection  
for an integrated circuit, comprising:

2      mounting an integrated circuit die on a lead frame;  
3      encapsulating at least part of the integrated circuit die  
4      with a plastic or epoxy material; and

5      folding a portion of the lead frame around sides of the  
6      encapsulated integrated circuit die and over or adjacent to a  
7      peripheral upper surface of the plastic or epoxy material.

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1. The method of claim 1, further comprising:

2      connecting the portion of the lead frame folded around  
3      the sides of the encapsulated integrated circuit die and over  
4      or adjacent to the peripheral upper surface of the plastic or  
5      epoxy material to a ground voltage.

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3. The method of claim 1, wherein the step of encapsulating  
7      at least part of the integrated circuit die with a plastic or  
8      epoxy material further comprising:

1      after mounting the integrated circuit die on the lead  
2      frame, encapsulating exposed surfaces of the integrated  
3      circuit die except for a sensing surface; and  
4      encapsulating wire bonds connecting the integrated  
5      circuit die to portions of the lead frame.

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4. The method of claim 1, wherein the step of folding a  
7      portion of the lead frame around sides of the encapsulated  
8      integrated circuit die and over or adjacent to a peripheral  
upper surface of the plastic or epoxy material further  
comprising:

1      folding portions of the lead frame around each side of  
2      the encapsulated integrated circuit die.

1       5. The method of claim 1, wherein the step of folding a  
2 portion of the lead frame around sides of the encapsulated  
3 integrated circuit die and over or adjacent to a peripheral  
4 upper surface of the plastic or epoxy material further  
5 comprising:

6             folding a first portion of the lead frame around a first  
7 side of the encapsulated integrated circuit die, wherein the  
8 first portion includes an opening providing access for a  
9 connector to pins electrically connected to the integrated  
10 circuit die.

1       6. The method of claim 1, wherein the step of folding a  
2 portion of the lead frame around sides of the encapsulated  
3 integrated circuit die and over or adjacent to a peripheral  
4 upper surface of the plastic or epoxy material further  
5 comprising:

6             folding portions of the lead frame around edges of the  
7 encapsulated integrated circuit die not including leads  
8 electrically connected to the integrated circuit die.

1       7. The method of claim 1, wherein the step of folding a  
2 portion of the lead frame around sides of the encapsulated  
3 integrated circuit die and over or adjacent to a peripheral  
4 upper surface of the plastic or epoxy material further  
5 comprising:

6             folding a first portion of the lead frame around a side  
7 of the encapsulated integrated circuit die; and

8             folding a second portion of the lead frame extending from  
9 the first portion over a peripheral upper surface of the  
10 encapsulated integrated circuit die.

1       8. The method of claim 1, wherein the step of folding a  
2 portion of the lead frame around sides of the encapsulated  
3 integrated circuit die and over or adjacent to a peripheral

4       upper surface of the plastic or epoxy material further  
5       comprising:  
6           folding a first portion of the lead frame around a side  
7       of the encapsulated integrated circuit die; and  
8           folding a second portion of the lead frame extending from  
9       the first portion adjacent to and level with a peripheral  
10      upper surface of the encapsulated integrated circuit die.

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- 1       9. An integrated circuit package, comprising:  
2           an integrated circuit die mounted on a lead frame; and  
3           a plastic or epoxy material encapsulating at least part  
4           of the integrated circuit die,  
5           wherein a portion of the lead frame is folded around  
6           sides of the encapsulated integrated circuit die and over or  
7           adjacent to a peripheral upper surface of the plastic or epoxy  
8           material.
- 1       10. The integrated circuit package of claim 9, further  
2           comprising:  
3           a connection between a ground voltage and the portion of  
4           the lead frame folded around the sides of the encapsulated  
5           integrated circuit die and over or adjacent to the peripheral  
6           upper surface of the plastic or epoxy material.
- 1       11. The integrated circuit package of claim 9, wherein the  
2           plastic or epoxy material encapsulates exposed surfaces of the  
3           integrated circuit die except for a sensing surface and wire  
4           bonds connecting the integrated circuit die to portions of the  
5           lead frame.
- 1       12. The integrated circuit package of claim 9, wherein  
2           portions of the lead frame are folded around each side of the  
3           encapsulated integrated circuit die.
- 1       13. The integrated circuit package of claim 9, wherein a  
2           first portion of the lead frame folded around a first side of  
3           the encapsulated integrated circuit die includes an opening  
4           providing access for a connector to pins electrically  
5           connected to the integrated circuit die.
- 1       14. The integrated circuit package of claim 9, wherein  
2           portions of the lead frame are folded only around edges of the

3       encapsulated integrated circuit die not including leads  
4       electrically connected to the integrated circuit die.

1       15. The integrated circuit package of claim 9, wherein:  
2            a first portion of the lead frame is folded around a side  
3            of the encapsulated integrated circuit die; and  
4            a second portion of the lead frame extending from the  
5            first portion is folded over a peripheral upper surface of the  
6            encapsulated integrated circuit die.

1       16. The integrated circuit package of claim 9, wherein:  
2            a first portion of the lead frame is folded around a side  
3            of the encapsulated integrated circuit die; and  
4            a second portion of the lead frame extending from the  
5            first portion is folded adjacent to and level with a  
6            peripheral upper surface of the encapsulated integrated  
          circuit die.

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- 1       17. An integrated circuit package, comprising:  
2            a lead frame including a die paddle and portions  
3            extending from the die paddle;  
4            an integrated circuit die mounted on the die paddle;  
5            a plastic or epoxy material encapsulating exposed  
6            surfaces of the integrated circuit die except for a sensing  
7            surface,  
8            wherein the portions of the lead frame extending from the  
9            die paddle ~~are~~ folded around sides of the encapsulated  
10          integrated circuit die and over or adjacent to peripheral  
11          upper surfaces of the encapsulated integrated circuit die.
- 1       18. The integrated circuit package of claim 17, wherein the  
2           lead frame includes pins or leads and the portions extending  
3           from the die paddle include openings around the pins or leads.
- 1       19. The integrated circuit package of claim 17, wherein the  
2           lead frame includes pins or leads and the portions extending  
3           from the die paddle project from peripheral edges of the die  
4           paddle not adjacent to the pins or leads.

1        20. A lead frame strip for an integrated circuit package,  
2        comprising:  
3                at least one lead frame, the lead frame including:  
4                a die paddle on which an integrated circuit will be  
5        mounted;  
6                a plurality of structures which will be formed into  
7        pins or leads for the integrated circuit package; and  
8                portions extending from the die paddle which will be  
9        folded around sides of the integrated circuit package and  
10      over or adjacent to a peripheral upper surface of the  
11      integrated circuit package to form an electrostatic  
12      discharge ring.

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